**In The Claims:**

Claim 1. (Currently amended) A data processing apparatus for executing multiple instruction sets comprising:

a memory, for storing a plurality of instruction words of the instruction sets;

a processor core, for executing a primary instruction word of the instruction words;

a program counter register (PC), for addressing a next instruction word stored in the memory;

a plurality of data registers, for storing data of the instruction words;

a processor status register, for storing a status of the processor core, wherein the processor status register contains an instruction set selector (ISS) for indicating a current instruction set of the instruction sets;

a predecoder, for translating at least one of the instruction sets to the primary instruction word and outputting therewith;

an Icache, for storing the primary instruction word;

a decoder, for decoding the primary instruction word, wherein the processor core is used for executing the primary instruction word decoded by the decoder;

a program counter control, responsive to the instruction set selector to modify the value of the program counter to fit the length of the instruction word, whose length is different from that of the primary instruction word; and

a bus, being an interface between the predecoder and the memory.

Claim 2. (Previously presented) The apparatus of claim 1, wherein there are two sets of bits in each of the data registers, at least one bit is viewed as an instruction set selection bit (IS) and the other bits stored in each data register are viewed as a target address (TA).

Claim 3. (Previously presented) The apparatus of claim 2, wherein the target address is a starting address of an instruction set.

Claim 4. (Original) The apparatus of claim 2, wherein the ISS is set by a specified branch instruction according to the IS in the data registers.

Claim 5. (Original) The apparatus of claim 1, wherein the predecoder contains at least one sub-decoder, for translating at least one of the instruction sets to the primary instruction word.

**Claims 6-7 (Cancelled)**

Claim 8. (Original) The apparatus of claim 1, wherein the instruction set selector includes at least one bit.

Claim 9. (Original) The apparatus of claim 8, wherein the instruction set selector can be set by a specified branch instruction according to one or more instruction set bits of the data registers.

Claim 10. (New) The apparatus of claim 1, wherein the predecoder contains a plurality of sub-decoders, and switching between the sub-decoders is controlled by the ISS.